Notice of Allowability	Application No.	Applicant(s)	
	10/797,727	JOBS ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 07/17/2007*.

2. ☒ The allowed claim(s) is/are *1, 3-12, 15-17, 19-30, 33-36, 39-47, 51-58, 61, 64-68, 71-73, 76-77, 82-84, 86-87, 90-93, 96-98, 104-118 and 121-122; renumbered as 1-86, respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TUAN V. THAI
PRIMARY EXAMINER

Continuation of Attachment(s) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 05/25/2007, 07/17/2007.

DETAILED ACTION

1. This Office Action is in response to the communication filed on 07/17/2007. None of the claims are amended, cancelled or newly added. Therefore, claims 1, 3-17, 19-44, 46-47 and 49-122 are currently pending in this application.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with Michael G. Pate (Reg. No. 53,439) on 09/14/2007.

4. The application has been amended as follows:

CLAIM 1 (Currently Amended):

In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a first communications path having a first ~~capacity~~ plurality of signal lines;
- coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a second communications path having a second

~~capacity~~ plurality of signal lines, where the sum of the first ~~capacity~~ plurality of signal lines and the second ~~capacity~~ plurality of signal lines is a fixed value; and

- altering the first capacity and the second capacity by transitioning at least one of the first plurality of signal lines from the first communications path to the second communications path or transitioning at least one of the second plurality of signal lines from the second communications path to the first communications path during the operation of the memory system based on the rate at which the signals are being coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which the signals are being coupled from the memory hub in the at least one memory module to the ~~module~~ memory hub controller.

CLAIMS 13-14 (Cancelled).

CLAIM 17 (Currently Amended):

In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having a M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling command, address and data signals in a downstream direction from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;
- coupling data signals in a upstream direction from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; and

- determining a first rate at which data signals are being coupled from the memory hub in the at least one memory module to the memory hub controller;
- determining a second rate at which command, address and data signals are being coupled from the memory hub controller to the memory hub in the at least one memory module;
- altering the values of N and P during the operation of the memory system based on the ~~rate at which signals are being coupled through the bus~~ first and second rates such that at least one of the signal lines of the bus transitions from coupling in the upstream direction to coupling in the downstream direction or from coupling in the downstream direction to coupling in the upstream direction.

CLAIM 19 (Currently Amended):

The method of claim 17 wherein the acts of determining the first rate and determining the second rate ~~altering the values of N and P~~ comprise:

- determining the first and second rates at the memory hub controller~~,~~ ~~determining the rate at which the signals are being coupled through the bus; and~~
- ~~altering the values of N and P based on the determined rate at which the signals are being coupled through the bus~~.

CLAIM 20 (Currently Amended):

The method of claim 17 wherein the acts of determining the first rate and determining the second rate ~~altering the values of N and P~~ comprise:

- determining the first and second rates at the memory hub ~~of the at least one memory module, determining the rate at which the signals are being coupled through the bus; and~~
- ~~altering the values of N and P based on the determined rate at which the signals are being coupled through the bus~~.

CLAIMS 31-32 (Cancelled).

CLAIM 36 (Currently Amended):

A memory system, comprising:

- a memory hub controller having M buffers, N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, the values of N and P being alterable during the operation of the memory system;
- at least one memory module, comprising a memory hub having a plurality of buffers, N of which are configured as input buffers and P of which are configured as output buffers; and
- a plurality of memory devices coupled to the memory hub; and
- a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, the value of M being equal to the sum of N and P and the values of N and P further being altered within a range of minimum and maximum values of N and P respectively according to a rate of data transfer from the memory hub controller to the at least one memory module and a rate of data transfer from the at least one memory module to the memory hub controller such that the sum of N and P remains constant and equal to M by either transitioning at least one of the output buffers to input buffers or transitioning at least one of the input buffers to output buffers.

CLAIMS 37-38 (Cancelled).

CLAIMS 39-41 (Currently Amended): CHANGE DEPENDENCY OF CLAIMS 39-41 (FROM CLAIM 37) TO CLAIM 36

CLAIM 47 (Currently Amended):

A processor-based system, comprising:

- a processor having a processor bus;

- a system controller coupled to the processor bus, the system controller having a peripheral device port;
- a memory hub controller coupled to the processor bus, the memory hub controller having an output port and an input port;
- at least one input device coupled to the peripheral device port of the system controller;
- at least one output device coupled to the peripheral device port of the system controller;
- at least one data storage device coupled to the peripheral device port of the system controller;
- at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub;
- a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus coupling first signals from the memory controller to the memory hub of the at least one memory module, the downstream bus having a width of M bits, the value of M being variable to adjust that bandwidth of the downstream bus and the value of M further being alterable based on the rate at which the first signals are being coupled from the memory controller to the memory hub of the at least one memory module~~through~~;
- an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, the upstream bus coupling second signals from the memory hub of the at least one memory module to the memory controller, the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus and the value of N further being alterable based on the rate at which the second signals are being coupled from the memory hub of the at least one memory module to the memory controller~~through~~; and
- wherein at least one of the memory hub controller and memory hub is operable to determine the rate at which the second and first signals are

being coupled through the upstream and downstream buses, respectively, and wherein memory hub controller is operable to alter the values of M and N based on the determined rate by either transitioning at least one of the M bits of the downstream bus to one of the N bits of the upstream bus or transitioning at least one of the N bits of the upstream bus to one of the M bits of the downstream bus.

CLAIMS 49-50 (Cancelled).

CLAIM 58 (Currently Amended):

In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity;
- coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value;
- altering the first capacity and the second capacity during the operation of the memory system; and
- configuring buffers in the memory hub controller and in the memory hub of the at least one memory module as either input buffers or output buffers;
- wherein the acts of altering the first capacity and the second capacity comprise
    - o determining the rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in

the at least one memory module based on the type of hardware included in a system associated with the memory system; and

- o altering the first capacity and the second capacity based on the determined rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module by transitioning at least one of the output buffers to input buffers or transitioning at least one of the input buffers to output buffers.

CLAIMS 59-60, 62-63 (Cancelled).

CLAIM 66 (Currently Amended):

In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity and comprising a plurality of signal lines;
- coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity and comprising a plurality of signal lines, where the sum of the first capacity and the second capacity is a fixed value;
- determining the rates at which it is anticipated that the command, address and data signals will be coupled from the memory hub controller to the memory hub in the at least one memory module and at which data signals will be coupled from the memory hub in the at least one memory module to the memory hub controller based on the type of hardware included in a system associated with the memory system; and

- altering the first capacity and the second capacity during the operation of the memory system based on the determined rate at which it is anticipated that the signals will be coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which it is anticipated that the signals will be coupled from the memory hub in the at least one memory module to the module memory hub controller by transitioning at least one of the plurality of signal lines from the first communications path to the second communications path or transitioning at least one of the plurality of signal lines from the second communications path to the first communications path.

CLAIMS 69-70 (Cancelled).

CLAIM 73 (Currently Amended):

In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity and comprising a plurality of signal lines;
- coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity and comprising a plurality of signal lines, where the sum of the first capacity and the second capacity is a fixed value; ~~and~~
- determining the rates at which the command, address and data signals are coupled from the memory hub controller to the memory hub and from the memory hub to the memory hub controller; and

- altering the first capacity and the second capacity during the operation of the memory system according to the determined rates within a range of minimum and maximum values for the first capacity and the second capacity respectively by transitioning at least one of the plurality of signal lines from the first communications path to the second communications path or transitioning at least one of the plurality of signal lines from the second communications path to the first communications path.

CLAIMS 74-75, 78-81 (Cancelled).

CLAIM 82 (Currently Amended):

In a memory system having a memory hub controller and at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, a method of coupling command, address and data signals between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling ~~signals in a packet that includes~~ command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity and comprising a plurality of signal lines;
- coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity and comprising a plurality of signal lines, where the sum of the first capacity and the second capacity is a fixed value; ~~and~~
- determining the rates at which the command, address, and data signals are coupled from the memory hub controller to the memory hub and data signals are coupled from the memory hub to the memory hub controller; and
- altering the first capacity and the second capacity during the operation of the memory system according to the determined rates by transitioning at least one of the plurality of signal lines from the first communications path to the second communications path or transitioning at least one of the plurality of

signal lines from the second communications path to the first communications path.

CLAIM 84 (Currently Amended):

In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having a M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;
- coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; ~~and~~
- determining a first rate at which the command, address and data signals are coupled from the memory hub controller to the memory hub;
- determining a second rate at which the data signals are coupled from the memory hub to the memory hub controller;
- altering the values of N and P during the operation of the memory system according to the first and second rates by ~~configuring~~ transitioning buffers in the memory hub controller and in the memory hub of the at least one memory module [[as]]from either input buffers [[or]]to output buffers or output buffers to input buffers.

CLAIM 85 (Cancelled).

CLAIM 86 (Currently Amended): CHANGE DEPENDENCY OF CLAIM 86 (FROM CLAIM 85) TO CLAIM 84.

CLAIMS 88-89 (Cancelled).

CLAIM 93 (Currently Amended):

In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having [[a]] M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling command, address and data signals in a downstream direction from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;
- coupling data signals in a upstream direction from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; ~~and~~
- determining a rate at which the command, address and data signals are coupled through the bus;
- altering the values of N and P during the operation of the memory system based on the determined rate such that at least one of the M signal lines of the bus transitions from coupling in the upstream direction to coupling in the downstream direction or from coupling in the downstream direction to coupling in the upstream direction, the values of N and P being within a range of minimum and maximum values of N and P respectively.

CLAIMS 94-95, 99-103 (Cancelled).

CLAIM 104 (Currently Amended):

In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having a M signal lines coupled between the memory

hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling ~~signals in a packet that includes~~ command, address and data signals in a downstream direction from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus;
- coupling data signals in a upstream direction from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M;
- determining a rate during operation at which the command, address and data signals coupled from the memory hub controller to the memory hub and data signals coupled from the memory hub in the at least one memory module to the memory controller are coupled through the bus; and
- altering the values of N and P during the operation of the memory system based on the determined rate such that at least one of the M signal lines of the bus transitions from coupling in the upstream direction to coupling in the downstream direction or from coupling in the downstream direction to coupling in the upstream direction.

CLAIM 107 (Currently Amended):

In a memory system having a memory hub controller, at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub, and a bus having a M signal lines coupled between the memory hub controller and the memory hub in the at least one memory module, a method of coupling command, address and data signals through the bus between the memory hub controller and the memory hub in the at least one memory module, the method comprising:

- coupling command, address and data signals in a downstream direction from the memory hub controller to the memory hub in the at least one memory

module using N of the M signal lines of the bus and further using a uni-directional downstream bus having N signal lines;

- coupling data signals in a upstream direction from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus and further using a uni-directional upstream bus having P signal lines, where N+P = M; and
- determining the rates during operation at which the command, address and data signals are coupled from the memory hub controller to the memory hub and at which data signals are coupled from the memory hub to the memory hub controller; and
- altering the values of N and P during the operation of the memory system according to the determined rates such that at least one of the M signal lines of the bus transitions from coupling in the upstream direction to coupling in the downstream direction or from coupling in the downstream direction to coupling in the upstream direction.

CLAIM 109 (Currently Amended):

A memory system, comprising:

- a memory hub controller having M buffers, N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, the values of N and P being alterable during initialization of the memory system;
- at least one memory module, comprising a memory hub having a plurality of buffers, N of which are configured as input buffers and P of which are configured as output buffers; and
- a plurality of memory devices coupled to the memory hub; ~~and~~
- a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, the value of M being equal to the sum of N and P; and
- wherein at least one of the memory hub and memory hub controller is operable to determine the rate at which signals are being coupled through

the bus, and wherein the values of P and N buffers for the respective buffers in the memory hub controller and the memory hub are altered based on the determined rate at which the signals are being coupled through the bus by transitioning at least one of the input buffers to output buffers or at least one of the output buffers to input buffers.

CLAIM 118 (Currently Amended):

A processor-based system, comprising:

- a processor having a processor bus;
- a system controller coupled to the processor bus, the system controller having a peripheral device port;
- a memory hub controller coupled to the processor bus, the memory hub controller having an output port and an input port;
- at least one input device coupled to the peripheral device port of the system controller;
- at least one output device coupled to the peripheral device port of the system controller;
- at least one data storage device coupled to the peripheral device port of the system controller;
- at least one memory module having a memory hub and a plurality of memory devices coupled to the memory hub;
- a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits, the value of M being variable to adjust that bandwidth of the downstream bus and the value of M further being alterable based on the rate at which it is anticipated that the signals will be coupled through at least the downstream bus; and
- an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus and the value

of N further being alterable based on the rate at which it is anticipated that the signals will be coupled through at least the upstream bus;

- wherein at least one of the memory hub controller and the memory hub of the at least one controller operable to
    - determine the rate at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module based on the type of hardware included in a system associated with the memory system; and
    - alter the values of M and N based on the determined rates at which it is anticipated that the signals will be coupled between the memory hub controller and the memory hub in the at least one memory module by transitioning at least one of the M bits of the downstream bus to the upstream bus or transitioning at least one of the N bits of the upstream bus to the downstream bus.

CLAIMS 119-120 (Cancelled).

Allowable Subject Matter

5. Claims 1, 3-12, 15-17, 19-30, 33-36, 39-47, 51-58, 61, 64-68, 71-73, 76-77, 82-84, 86-87, 90-93, 96-98, 104-118 and 121-122 are allowed; and they are renumbered as 1-86, respectively.

REASONS FOR ALLOWANCE

6. The following is an examiner's statement of reasons for allowance:

When considered with all of the other limitations, the prior art of record does not teach or suggest, either alone or in combination, **all** the limitations of the amended claims of the current invention (renumbered independent claims 1, 14, 30, 38, 46, 50,

55, 58, 60, 66, 70, 73, 75 and 84); particularly about altering the input and output capacities/bandwidths of the communication path connecting a memory hub controller and a memory hub in the at least one memory module, by transitioning at least one signal line from input direction to output direction or vice versa, based on the rate of the actual or anticipated signal flow through the communication path.

Bisson et al. (USPN: 7,136,953) disclose a bus/link having a variable bandwidth which can be adjusted to less than or equal to the maximum bandwidth as needed. However, unlike the instant invention, Bisson's bus/link cannot transition at least part of the bandwidth from one direction to other.

Renumbered claims 2-13, 15-29, 31-37, 39-45, 47-49, 51-54, 56-57, 59, 61-65, 67-69, 71-72, 74, 76-83 and 85-86 further limit the allowable independent claims. These claims are therefore allowable for the same reason as set forth supra.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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TUAN V. THAI
PRIMARY EXAMINER